

FIG. 1

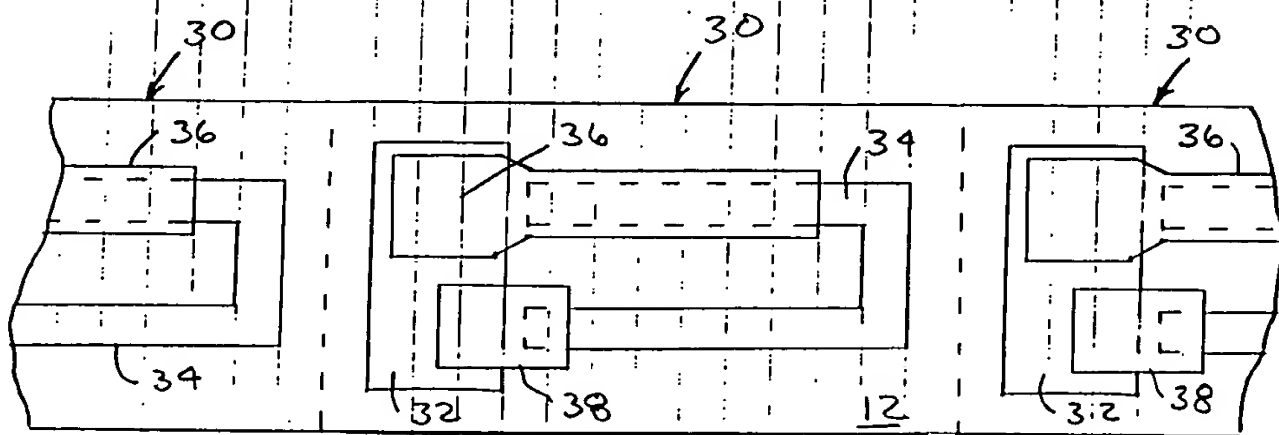


FIG. 2

A schematic diagram of a parallel processing system 500. It features two parallel horizontal paths. The top path starts with a circular input 52, followed by a series of two pairs of circles (56 and 60) stacked vertically, each pair connected to a rectangular block. This is followed by a rectangular block 64. The bottom path starts with a circular input 54, followed by a series of two pairs of circles (58 and 62) stacked vertically, each pair connected to a rectangular block. This is followed by a rectangular block 66. The outputs of blocks 64 and 66 are connected to a junction point 68. From junction 68, a line leads to a pair of circles 70, which then connects to a rectangular block 72. The output of block 72 is connected to a final output 80, represented by a series of horizontal lines.

A cross-sectional view of a multi-layered structure 80. The structure consists of a top layer 52, a middle layer 82, and a bottom layer 54. The middle layer 82 contains a central rectangular region 84. This region 84 is further divided into two horizontal sub-regions: a top sub-region 86 and a bottom sub-region 88. The sub-region 86 is filled with a stippled pattern, while the sub-region 88 is filled with a cross-hatched pattern. The entire structure 80 is shown within a frame that has a wavy, irregular boundary on the left and right sides.

FIG. 4

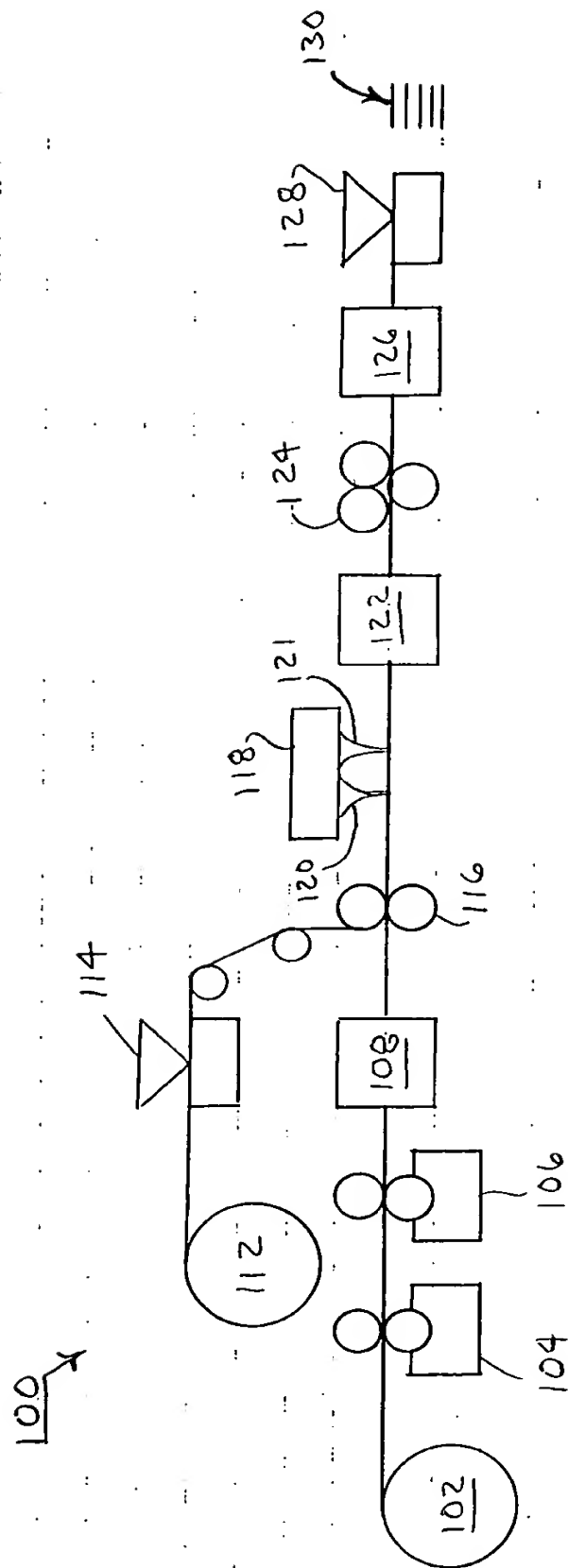


FIG. 5

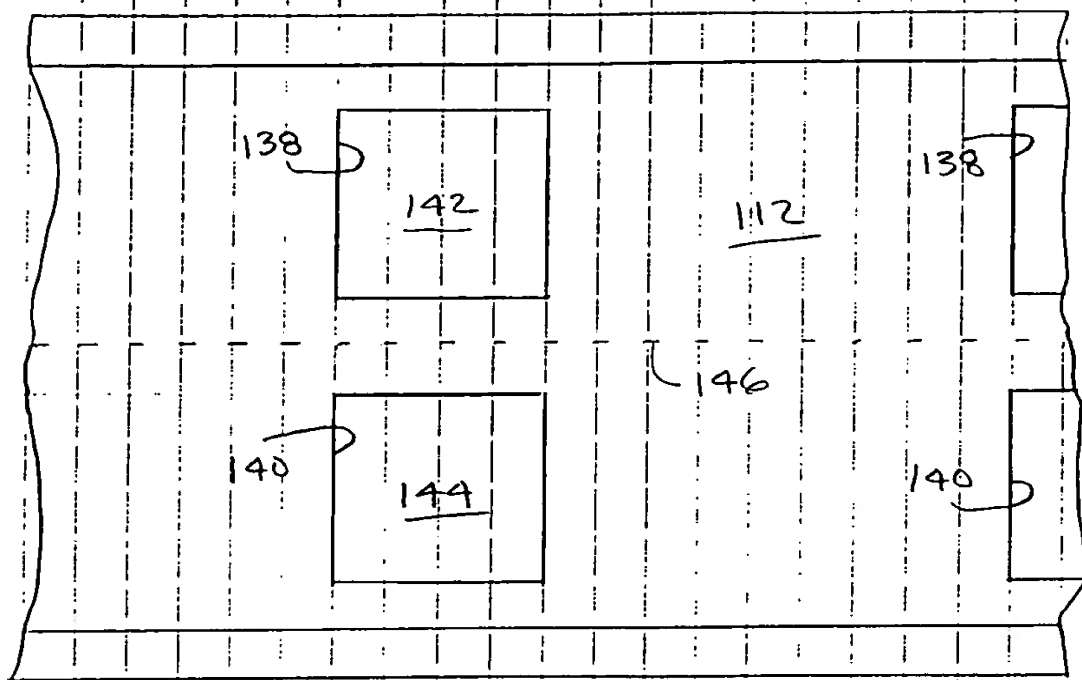


FIG. 6

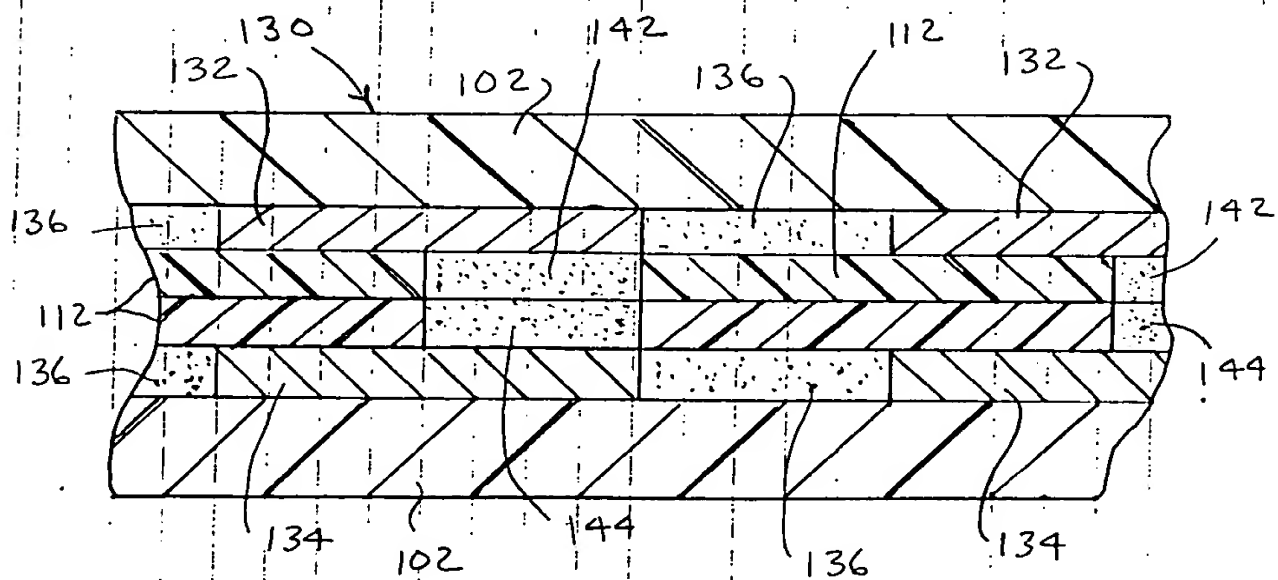


FIG. 7